AMENDMENT TO THE CLAIMS:

Please cancel claims 1, 2 and 19 without prejudice or disclaimer of the subject matter and amend claims 3, 4 and 20 as follows:

Claim 1-2 (Cancelled).

3. (Currently Amended) ~~The~~ A clock synchronizer ~~according to claim 2, wherein~~ generating a second clock signal synchronized with a first clock signal, comprising:

a phase difference detection circuit detecting a phase difference between said first and second clock signals, and setting a first control signal to be at an activated level for a time period corresponding to the phase difference;

a loop filter connected to a predetermined node;

a current-supply circuit supplying current to said loop filter in response to the first control signal from said phase difference detection circuit; and

a clock generating circuit generating said second clock signal in accordance with a potential of said predetermined node; wherein

said current-supply circuit includes

a variable current source whose output current can be controlled,

a first switching circuit passing output current of said variable current source through said loop filter in response to that said first signal is set to be at the activated level, and

a first control circuit controlling said variable current source such that predetermined constant current flows from said variable current source to said loop filter, based on the potential of said predetermined node,

wherein:

said variable current source includes a first transistor of a first conductivity type whose input electrode receives a first control potential,

said first switching circuit connects said first transistor between a line of a first power-supply potential and said loop filter in response to that said first control signal is set to be at the activated level, and

said first control circuit controls said first control potential such that predetermined constant current flows through said first transistor connected between the line of said first power-supply potential and said loop filter, based on the potential of said predetermined node,

said first control circuit ~~(7, 8, 50, 51)~~ including ~~includes~~

a second transistor ~~(21, 26)~~ of a first conductivity type whose first electrode is connected to the line of said first power-supply potential ~~(VCC, GND)~~, and whose input electrode is connected to a second electrode of said second transistor, and outputting said first control potential ~~(VCP, VCN)~~ from the second electrode,

a third transistor ~~(22, 25)~~ of a second conductivity type whose first electrode is connected to a second electrode of said second transistor ~~(21, 26)~~ and whose input electrode receives the potential ~~(VC)~~ of said predetermined node, and

a first resistance element ~~(23, 24)~~ connected between a second electrode of said third transistor ~~(22, 25)~~ and a line of a second power-supply potential ~~(GND, VCC)~~.

4. (Currently Amended) The clock synchronizer according to claim 3, wherein said first control circuit ~~(50, 51)~~ further includes a second resistance element ~~(52, 53)~~ connected between the second electrode of said second transistor ~~(21, 26)~~ and the line of said second power-supply potential ~~(GND, VCC)~~.

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Claims 5-18 (Withdrawn)

Claim 19 (Cancelled)

20. (Currently Amended) A clock synchronizer generating a second clock signal ~~(FCLK)~~ synchronized with a first clock signal ~~(RCLK)~~, comprising:

a phase difference detection circuit ~~(1)~~ detecting a phase difference between said first and second clock signals ~~(RCLK, FCLK)~~, and setting a control signal ~~(UP, DOWN)~~ to be at an activated level for a time period corresponding to the phase difference;

a loop filter ~~(9)~~ including a resistance element ~~(10)~~ and a capacitor ~~(11)~~ connected in series between a predetermined node and a line of a reference potential ~~(GND)~~;

a current-supply circuit ~~(2, 7, 8, 41, 80, 86, 87, 110, 113)~~ supplying current to said loop filter ~~(9)~~ in response to ~~a~~ said control signal ~~(UP, DOWN)~~ from said phase difference detection circuit ~~(1)~~; and

a clock generating circuit ~~(12, 13, 40)~~ generating said second clock signal ~~(FCLK)~~ in accordance with a potential ~~(VC)~~ of said predetermined node;

said current-supply circuit ~~(2, 7, 8, 41, 80, 86, 87, 110, 113)~~ including

a transistor ~~(3, 6)~~ whose input electrode receives a control potential ~~(VCP, VCN)~~,

a switching circuit ~~(4, 5, 82, 83)~~ connecting said transistor ~~(3, 6)~~ between a line of a power-supply potential ~~(VCC, GND)~~ and said loop filter ~~(9)~~, in response to that said control signal ~~(UP, DOWN)~~ is set to be at an activated level, and

a control circuit ~~(7, 8, 86, 87)~~ controlling said control potential ~~(VCP, VCN)~~ such that predetermined constant current flows through said transistor ~~(3, 6)~~ connected between the line of said power-supply potential ~~(VCC, GND)~~ and said loop filter ~~(9)~~, based on a potential ~~(VC')~~ of a node between said resistance element ~~(10)~~ and ~~a~~ said capacitor ~~(11)~~.